Basic Language Elements

Data Declarations

```
signal carryIn : std_logic;
signal tripleSwitch : std_logic_vector(2 downto 0);
signal dataBus : std_logic_vector(15 downto 0);
```

Data Assignment

```
carryIn <= '1';
tripleSwitch <= "001";
tripleSwitch(1) <= '1';
dataBus <= X"000F";          here the X identifies a hexadecimal number
dataBus <= "0000000000001111";
```

Dataflow Model – Concurrent Statements

Conditional Signal Assignment

```
signal <= value1 when condition else
          value2 when condition else
          value3;
```

```
op <= inA when sel = '1'
          else inB;
```

see also ***ISE_ALU.vhd***

Process – Sequential Statements

If – then – else

```
if condition1 then
   statement1;
elsif condition2 then
   statement2;
else
  statement3;
end if;
```

```
if rising_edge(clk) then
  if load = '1' then
    data_out <= data_in;
  end if;
end if;
```

Case

```
case expression is
  when choice1 => statements;
  when choice2 => statements;
end case;
```

```
  case state is
    when stateA =>
      if(KDU = "101") then
        state <= stateB;
      end if;

    when stateB =>
      if(KDU(2) = '0') then
        state <= stateA;
      end if;
  end case;
```